Hot Embossing of LCP using Silicon Master Tool for Short Distance Optical Interconnects

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ABSTRACT

A novel method has been developed for using 45° mirror surfaces for the vertical coupling of light into a channel for short distance optical interconnects. The method includes the structuring of silicon (100) wafer to act as a master tool, then using anisotropic etching followed by hot embossing of the master tool onto a desired substrate, in this case Liquid Crystal Polymer (LCP). In this paper, the process flow to develop such a master tool is discussed, followed by an explanation of the process of hot embossing the master tool onto the LCP. Free space light transmission is shown in the stamped LCP substrate in a channel which is 8 cm long and ~60 micrometer deep.

Keywords: 45° etching of silicon, hot embossing, optical interconnects, master tool, and vertical coupling

1. INTRODUCTION

Advancements in processor technology have introduced the possibility of data transmission rates of up to several gigabytes per second [1]. At these rates, conventional metallic interconnects exhibit higher crosstalk and attenuation, thereby limiting channel density and having high power dissipation [2]. Optical interconnects can be a solution to these problems [2]; however, there are technical challenges that need to be overcome to make way for board level optical interconnects. Several methods and techniques, most of which are waveguide based, have also been developed for board level optical interconnects [2] – [6].

Additionally, several challenges need to be overcome when integrating optic components into a circuit board. VCSELs (Vertical cavity surface emitting lasers) and optical detectors are commonly used as sources and detectors, respectively, for short distance optical interconnects. Light from VCSEL must be directed at 90° in order to couple to the optical channel or interconnect as shown in Fig. 1.

Fig. 1. Schematic of an optical interconnect

Different methods, such as implanting a 45° mirror [2] [3], using tilted gratings [4], fabricating 45° micromirrors with the soft molding technique [5], cutting the waveguide by a microtome blade [6], etc. have been used to overcome this required 90° bend. In this paper we introduce a new method of coupling the light from the light
source to the optical channel over this 90° bend has been developed using silicon master tool to hot emboss surfaces onto a LCP substrate. In developing this method, previously discovered techniques of anisotropic etch of silicon for 45° surfaces [7] are implemented to micromachine the silicon wafer. An alternative method to create 45° surfaces is also discussed in reference [8]. The hot embossing technique [9] typically uses the etched silicon wafer to stamp the substrate. This particular method of hot embossing is compatible with current integrated circuit fabrication technology and is also mass producible.

2. PROCEDURE

2.1 Approach

The method for developing short distance optical interconnects can be divided into two steps. The first step is the fabrication of a master tool (MT), and the second step is the hot embossing with the fabricated MT on a polymer substrate. The MT can be of any material, as long as it has reasonable surface roughness. Because anisotropic etching can be easily rendered in silicon, etched silicon can be used as an MT. Figure 2 shows the steps of the fundamental process flow for making optical interconnects using silicon etching and hot embossing.

Figure 2 (b) shows silicon oxide thin film acting as a mask for the bulk micromachining of the silicon substrate. The etched planes can be arranged for 54.74° or 45° to the substrate; thus realizing two possibilities for fabricating MTs with anisotropic etching. Figure 2 (c) depicts an MT that is now ready for the hot embossing step. The hot embossing of the MT on the LCP occurs when the temperature is above the molding temperature of the LCP. Figure 2 (d) shows the sputtered aluminum needed on the hot embossed channel for optical reflectivity. The optical interconnect can be made as a free space or a core-cladding waveguide based.

![Fabrication process developed for optical interconnects](image-url)
2.2 Process flow to fabricate the master tool

In order to produce the desired MT for imprinting onto a substrate, two different surfaces are required. This desired MT contains 45° surfaces at the entry and exit positions of the waveguide device, and vertical walls along the length of the device. Process steps for fabrication of a Y-splitter are described by figures 3-7. The process flow for all other waveguide devices such as 1×4 and STAR splitter follow similar procedure. This process flow uses three masks. The first mask has a few tiny circular holes to etch (111) planes in (100) silicon wafer, giving an angle of 54.74° between these planes. The basic purpose of this mask is simply the alignment of the subsequent masks and wafer.

The second mask is shown in Figure 3. It contains a rectangle which is oriented at a 45° angle from the horizontal so that it is 45° from the (110) primary flat of the (100) silicon crystalline planes of which is one of the requirements to realize 45° surfaces in silicon [7]. This mask also defines the length of the Y-splitter device. In this process flow silicon was etched three times using silicon oxide as a mask. The process flow figures show a top view of the wafer at different stages.

Figure 4 shows a (100) Si wafer with 45° orientation of its primary flat with respect to the rectangle. The bulk micromachining of the 45° surfaces occur at all four edges of the rectangle.

Mask 3 is the Y-splitter mask given in Figure 5. The Y-splitter is also inclined by 45° from the horizontal because etching of the vertical walls in silicon requires the mask edge to be oriented at 45° from the (110) flat of the (100) silicon wafer [7].
A silicon oxide layer is grown again before using the mask 3 for the Y-splitter etch step. This ensures protection of the etched 45° mirror surfaces during the second etching step for the vertical walls. Figure 6 shows the wafer after patterning the oxide using mask 3. The wafer is now ready for vertical wall etching step.

Figure 7 shows the complete master tool with 45° surfaces at the entry and exit positions of the Y-splitter device and vertical walls along the length of the device. Only reactive ion etching can be used in the second step for vertical etching as the angle of split will be different if done by chemical etching. The masks 1 and 2 are designed in LASI and shown in Figures 8 and 9. Figure 8 is the LASI layout of mask 2 which contains devices of different lengths while figure 9 is the LASI layout of mask 3 which contains straight channels with 1×2, 1×4 and STAR splitters.
Using these masks and the process flow described previously, different MTs are produced and hot embossed. An MT with a straight channel of width ~200 µm is shown in Figure 10 with its zoomed view shown in Figure 11.
2.3 Hot embossing

After the fabrication of the MT, the next step is the hot embossing of the MT onto the substrate (LCP). Several attempts were made to achieve a quality hot embossing of waveguide patterns onto the LCP substrate using the silicon MT. To perform hot embossing the LCP substrate is sandwiched between the MT and a second silicon wafer and then is placed on the hot plate under the pressure of stacked iron bars. A thin coating of hydrophobic layer of DuPont is applied to the surface of the MT to avoid stiction of the LCP onto the MT. The hot plate is maintained at 380°C. This provided a temperature of 300°C at the top of the MT i.e. a temperature slightly above the molding temperature of the LCP. MTs are embossed keeping this temperature value at the top of the hot plate with the total weight pressure of the iron bars at 65 ± 0.5 kg. After the hot embossing, an aluminum layer of only a few microns thick is sputtered on the LCP in a standard sputtering chamber. This produced a typical free space channel with dimensions of 8 cm long, 200 µm wide, and a depth of 60 µm with 45° surfaces acting as micromachined mirrors.

3. RESULT

A He-Ne laser is incident on one of the 45° mirrors (top image in Fig.13) of an 8 cm long straight channel and then the reflected beam is observed at the second mirror/edge (bottom image in Fig.13). The free space light transmission through the hot-embossed channel using 45° edges on either end is shown in Fig.13. The light transmission is observed in all channels as well as for 2 and 4 cm long waveguides (shown in the LASI layout of mask 2 in Fig. 7). Only one 8 cm long straight channel is found to have observable light transmission at the other end.
4. CONCLUSION

One of the main challenges in realizing board level optical interconnects is the 90° bend required inside the substrate that connect the source and the detector. In this paper, a novel method for fabricating optical waveguides for PCB has been proposed and demonstrated. Furthermore, we have considered that the method chosen for manufacturing of optical interconnects should be mass producible and compatible with PCB fabrication technology. This method has several advantages, since embossing is a mass producible method, especially in comparison to cutting waveguides technique by a microtome blade mentioned in reference 6.

REFERENCES