Wafer-Level Micro/Nanosystems Integration and Packaging

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ABSTRACT
Micro nanosystems have attracted considerable interests and seen significant advances over the years. The huge gap between technology development and commercialization can be largely attributed to the challenges faced in the integration and packaging of the devices. The packaging has to work around the diverse functional requirements while ensuring that the device is able to perform effectively and reliably at the prescribed operating environments. The trend to make products lighter, smaller and thinner is relentless; heavy emphasis is placed on user friendliness, functionality, durability and price competitiveness. Wafer bonding is recognized to be a key technology for three dimensional (3D) integration and packaging; particularly for micro nanosystems that require vacuum packaging and hermetic sealing. The bonding process can be applied to a wide range of materials including silicon III–V semiconductor compounds, glass and ceramics. Low temperature bonding offers crucial advantages in multifunctional systems packaging such as system in packages (SiPs). Low temperature bonding through via interconnection metal to metal joining alignment and hermeticity are a set of process challenges that have to be collectively overcome before we are likely to see pervasive applications of micro nanosystems.

1. Introduction
The trend in micro nanosystems is to be lighter, smaller and cheaper. At the same time, there is a prodigious push for increasing functionalities. Such demands can only be fulfilled by progressively higher density integrated devices and circuits. Currently, high density packages can be single chip packages, multichip modules and 3D stacked packages. A significant portion of today’s IC packages still have low pin counts of below. Such requirements are easily met by low cost and reliable quad flat packages (QFPs), thin small outline packages (TSOP), and other peripheral lead surface mount packages. For higher pin counts, it is necessary to consider ball grid array (BGA) packages. To achieve yet higher chip density, the interconnections have to be shorter for better signal integrity and compactness. In this genre, chip scale packages (CSPs), flip chips and wafer level packages (WLPs) have been developed in recent years. Such packages are found in processors, mobile communication devices, and sensors. Further miniaturization and performance enhancement are obtained with multichip modules which combine multiple chips on a common platform or within a package. However, these packages are largely two-dimensional structuresconstituting the x, y direction with multiple chips mounted on a planar substrate.

Most of the current approaches in components packaging focus on single chip packages, but do not generically support the generation of maximum miniaturization for more complex systems integrating not only ICs but also sensors, microelectromechanical systems (MEMS), nanoelectromechanical systems (NEMS), devices, bus interfaces etc. Furthermore, increasing drive for the integration of disparate signals (digital, analog, RF, and technologies) in SOI, SiGe HBTs, GaAs, etc. can neither be supported by a system on a chip (SoC) concept nor any single IC fabrication technology.

2. MEMS/NEMS Packaging
Microelectromechanical systems (MEMS) call for the integration of components dealing with a myriad of phenomena such as motion, light, sound, chemical detection, radio waves, and computation. Examples of these commercialized MEMS devices include pressure sensors, inertial sensors, chemical sensors, optical MEMS, radio frequency (RF) MEMS, microfluidic MEMS, power MEMS, and bio MEMS [4]. Although fabrication techniques can be carried over from IC to MEMS fabrication, there are major differences in the requirements of MEMS packaging. MEMS NEMS packaging is widely acknowledged to be one of the most significant areas of research enabling more pervasive use of MEMS products. It is vital to explore and understand the possibilities and limitations of MEMS packaging and reliability.

MEMS NEMS packaging can be classified into two very different approaches; at the device level and at the wafer level [5, 7]. Device level packaging is not just time consuming, but also expensive. Wafer level packaging and protection of MEMS structures during wafer fabrication opens up the possibility for low cost packaging and also the enhancement of the functionality and reliability. Significant cost savings can be achieved if the wafer level packaged device is kept as similar to microelectronics chips as possible. These factors will improve and speed up the commercialisation potential. Typically, wafer level MEMS NEMS packaging process consists of wafer bonding, wafer thinning, interconnection planarisation, hermetic or non-hermetic sealing and assembly. Fig. illustrates a typical wafer level MEMS packaging processes using pressure sensor as a packaging example. The process flow includes:

[Additional text or content can be added here if needed]
3. 3D Integration and Packaging

To minimize the footprint and the signal transmission path, three dimensional (3D) packages or system in packages (SIP) with multiple vertically stacked chips are emerging. These packages exploit the z direction to more effectively increase the packaging density and incorporate additional functionalities to the integrated package. There are two distinct 3D stacking approaches as shown in Fig. One approach is to package the chips and then vertically stack these packages together using solder balls or bended leads. 3D packages using this approach include stacked TSOP, BGA, and tape chip packages (TCP). The chip connections with each single chip package include wire bonding, lead bonding, tape automated bonding (TAB), and flip chip bonding. Another approach is to first stack bare chips on top of one another and then use wire bonding, lead bonding, solder bumps or thin film routing to provide the vertical interconnections to the interposer supporting the chip stack. 3D heterogeneous integration allows the integration of Si III V Si Ge and MEMS devices into a single system. This yields a low cost solution and yet offers good electrical performance, high heat dissipating capability, and a mechanically stable structure that is able to withstand high environmental stresses.

Each of these approaches has inherent advantages and disadvantages. Generally, each lacks the flexibility to accommodate the wide range of chip dimensional and thickness variations found in stacked packages. There are also numerous technical challenges such as known good die testing, pad location constraints, poor horizontal routing, and the inability to rework.

Currently, 3D integration and packaging require some form of circuit redistribution under bump metallization, soldering, interposer and underfill or encapsulation. These secondary processes add to the manufacturing costs. Very high density micro-nano systems present challenging problems due to limitations in the pitch size possible with current techniques.
4. Novel Wafer-Level Micro/Nanosystems Packaging

Microsystems are invariably designed as systems with discrete components each with a specific function. Ideally all the components should be integrated and packaged together to form a product that is able to deliver the various functions. Such a situation can be realized with the use of a novel wafer level packaging and wafer bonding techniques.

Wafer bonding is likely to become a key technology for materials integration. MEMS NEMS packaging three dimensional (3D) integration and packaging as well as vacuum packaging and hermetic sealing. It is applicable to a wide range of materials including Si III–V semiconductor compounds glass and ceramics. The needs for interposition circuit redistribution under bump metallization soldering adhesive underfill or encapsulation can be obviated or minimized as the micro nanosystems can be directly integrated and packaged at the wafer level.

With the novel 3D integration and packaging scheme, multiple devices and micro nanosystem wafers are sequentially bonded to one another using wafer bonding and metal metal bonding. All the active layers are electrically interconnected using high aspect ratio vias filled with a metallic conductor. The bonded wafers would have multiple Al or Cu metal layers and interlevel dielectrics. Thus requiring low temperature bonding below 45°C to avoid metal degradation. As Cu wiring is widely used, this limits the processing temperatures to below 45°C. Otherwise, Cu will diffuse through the barrier layers and the reliability and thermal stability of material interfaces would deteriorate significantly. It is important to understand how to connect the active layers or devices with a reliable and compatible process. To achieve good bonding, the device and micro nanosystem wafer surfaces have to be mirror finish quality. Chemical mechanical polishing (CMP) of the to be bonded wafer surfaces is necessary prior to bonding. An existing or applied silicon oxide thin film is preferred to facilitate the simultaneous bonding of wafer-to-wafer and metal to metal. Fig. 3 illustrates the proposed 3D system. Three system layers are bonded and electrically interconnected using wafer wafer and metal metal bonding. It can be seen that the wafer wafer and metal metal bonding play an important role in the systems integration and packaging.

5. Wafer Bonding

Wafer bonding generally refers to a process by which two wafers fuse and adhere to each other when they are put into close contact. From the first systematic investigation of room temperature adhesion between two optically polished glass plates performed in 93 by Lord Rayleigh [1] the wafer bonding technique has been studied for several decades. It started with the manufacture of MEMS [2] mostly for automotive applications. Microsystems such as accelerometers, micromirrors, and gyroscopes require a sealed microcavity to protect the device from harsh environments while allowing the mechanical function to be realized. Other devices such as infrared (IR) detectors or resonant devices require a vacuum sealed package. Beyond MEMS and NEMS, other devices also drive wafer bonding technology; silicon on insulator (SOI) wafers [4] high performance microelectronics (such as high performance partially depleted and fully depleted CMOS [5]) double gate CMOS [6] and 3D device integration [7] photonics and optoelectronics [8] and monolithic integration [9]. The myriad of applications has led to the development of several bonding methods (Fig 4). The bonding process is applied to a wide range of materials including silicon III–V semiconductor compounds glass and ceramics.

These techniques can be categorized into direct bonding, anodic bonding, and intermediate layer bonding:

Direct bonding (fusion bonding): In direct bonding, two wafers are contacted without the assistance of any significant pressure, electrical fields, or intermediate layers [9]. This bonding technique usually leads to strong bonds and is widely used in silicon on insulator (SOI) technology.

Anodic bonding: It is based on the joining an electrical conducting material (e.g., silicon) and a material with ionic conductivity (e.g., alkali containing glass [10]). Anodic bonding usually leads to strong and hermetic bonds and is widely used for microsensor fabrication and for hermetic sealing of micromachined devices.

Intermediate layer bonding: Several low temperature bonding methods utilizing intermediate layers including metal, glass, or organic compounds of variable thickness have been reported in recent years [4]. Since it is usually less demanding on surface topography and cleanroom environment, intermediate layer bonding has been used in some special fields such as optically pumped VCSELs [5] and chemical analysis devices [6].
5.1 Direct Bonding

For room temperature wafer bonding in air the bonding energy is usually very low because the attraction between the pair is the van der Waals force and hydrogen bond [7]. In order to allow the bonded wafer pairs to sustain further wafer processes such as lapping thinning and patterning they have to be annealed at elevated temperatures after the room temperature bonding to enhance the bonding strength. However, the high temperature post annealing used in the bonding process will limit the applications of wafer bonding, especially in the bonding with processed wafers as follows [8-9]: thermal induced mechanical stress in bonding of materials with different thermal expansion coefficients undesirable changes and reactions in the case of materials and structures which are sensitive to high temperatures and occurrence of precipitates of oxides and vacancies at the bonded interface during heat treatment.

Therefore, it is crucial to achieve strong bonding by low temperature annealing. Up to now, there are a number of studies which are aimed at the development of methods that can yield strong bonding at low temperature or even at room temperature [3, 38].

One effective approach is to use dry or wet methods to activate the wafer surfaces after cleaning and before the room temperature bonding. In some cases, the cleaning and activation process may be combined. The cleaning treatment such as RCA cleaning also activates the bonding surfaces. A DHF solution treatment to enhance the low temperature bonding energy of thermal oxide covered wafer bonding has been reported [3]. It was also found that surface activated by dipping in hot nitric acid [37] or in hot NH₃OH solution [38] can effectively enhance the bond strength at low temperature as compared to that treated only in standard RCA solution.

Surface treatment by plasma exposure has also been shown to demonstrate the ability to enhance the bonding energy for wafer bonding [33, 35]. An amorphous surface layer on silicon wafers which was prepared by Ar ion implantation or thin film sputtering deposition was proved to enhance the bonding energy dramatically [3].

It was found that boron doped surface layer (produced by Boron Ion Implantation or treatment by B H plasma) can enhance the hydrophobic bonding energy [3, 3]. The mechanism is believed to be due to the effect of the neighbouring boron which appears to weaken the Si-H bonds leading to a reduction in the activation energy due to the release of hydrogen from the trapping centre [39 4]. However, one dissimilar layer with affluent boron will be produced which may cause problems in VLSI application.

Vacuum wafer bonding is another way to achieve high bond strength at low temperature. Tong et al. [3] found that low vacuum improves the bond strength at low temperature. The improvement is believed to be due to the acceleration of out diffusion of water and inert gas trapped at the interface by the vacuum at low temperatures. Bonding conducted under ultra-high vacuum (UHV) is also very attractive for bonding wafers without native oxide [3]. For in situ bonded pair of thermally cleaned hydrophilic silicon wafers under UHV, covalent bonds have been achieved at room temperature [3]. Very strong bonds have also been achieved at room temperature for silicon and gallium arsenide with the wafers cleaned and activated by an argon fast atom beam under UHV and in situ bonded under an external pressure akin to plasma treatment [4]. UHV wafer bonding usually requires preheating (~250°C) of the wafers prior to bonding or application of pressure during bonding in addition to the UHV conditions. This is costly in the mass production [4].

To achieve low temperature Si/Si, Si/SiO, SiO and Si/SiO bonding, medium vacuum bonding was employed in our studies [4, 44]. With careful control of the cleaning process and bonding process direct bonding at temperature of 450°C and varied applied loads, bond efficiency of above 99% and bond strength of above 200 MPa have been obtained. The scanning acoustic microscopy (SAM) micrographs of the directly bonded wafers are shown in Fig. 5. The bubble size, bubble number and the percentage of the unbonded area increase with an increase in the applied load. High applied loads keep the two wafer surfaces in tight contact at the early stage of wafer bonding. If there are impurities such as gases, water molecules and water...
rings are entrapped during bonding process the tight contact prevents them from escaping from the bonding interfaces with the result that bubbles and or cavities are formed

![Fig 5 C SAM micrographs of the bonded wafers under different applied loads at temperature 4 °C annealing time h and vacuum 10^-3 mbar (black area is bubble) (a) Applied load of 2 kN; (b) applied load of 3 kN; (c) applied load of 4 kN; and (d) applied load of 5 kN](image)

The applied loads have an effect on the bond strength (see upper curve in Fig 5). A higher applied load results in a lower bond strength. The bonded pairs have the highest bond strength when no load is applied. In all cases of vacuum wafer bonding, the bond strengths are above 9 MPa which is high enough for practical applications such as dicing and device fabrication.

![Fig 5 Comparison of bond strength under different loads](image)

5.2 Intermediate Layer Bonding

Normally direct wafer bonding requires very smooth and clean wafer surface. Hence high vacuum equipment are required for direct bonding. Intermediate layer bonding techniques have been developed for low temperature wafer bonding because of the less stringent requirements of the surface topography and cleanroom environment. Various low temperature wafer bonding processes using intermediate layers have been reported such as with intermediate layers of sodium rich glass [45, 46], metal [47, 49] and polymer [50, 51]. The intermediate layers have been deposited on the wafer surface with thicknesses in the range of several microns. For polymers, sodium ions can degrade the performance of electronic devices and the thermal stability of polymers can be problematic if subsequent processing stages require heat treatment at elevated temperatures. Metal intermediate layers increase the difficulty of leading out the electrical circuit from a sealed cavity. Besides these techniques may generate problems such as outgassing, low positioning accuracy, poor long term reliability and uncertain bond quality.

To avoid the above problems, sol gel amorphous silica layers can be used. Furthermore, there are several advantages. Firstly, sol gel processing is essentially a low temperature process as the conversion of Si OH groups into Si O Si units can occur at low temperatures [52, 54]. Secondly, it is possible to deposit a thin, uniform and homogeneous layer of amorphous silica on the substrates. This effectively smoothen the initial wafer surface and enables rough surfaces to be bonded. Thirdly, the sol gel films can be coated both inside or outside of complex shapes over large areas. Finally, sol gel processing is simple and low cost [55].

Sol gel intermediate layer bonding is attractive in the applications such as transferring a CMOS circuit to a foreign substrate combining MEMS and microelectronic circuits on silicon combining photonic devices such as lasers and detectors with driver or amplifier circuits or monolithic integration which describes the integration of disparate devices onto a single chip [56]. The devices inside the wafers usually cannot endure high temperatures and high voltages which is used in direct bonding and
anodic bonding respectively. Sol gel intermediate layer bonding can provide a stable and insulated interlayer for these applications.

Some research results on sol gel intermediate layer bonding have been reported [57 59]. Si to Si bonding has been achieved at a temperature of 3 °C [ ] as shown in Fig 7. Prior to bonding, the sol gel coating is annealed at different temperatures. The bonded area for room temperature annealing is about 55% and that for 75 °C annealed sol gel bonding is about 90%. The low bonding areas are due to the incomplete depletion of the residual organic species in sol gel intermediate layer. The bond efficiency of sol gel bonding is improved to about 85% with an annealing temperature of 3 °C. Similar results are obtained using an annealing temperature of 5 °C. The bond strength of annealed sol gel bonding is increased to about ~ 8 MPa when the annealing temperature is as high as 5 °C.

![Bond efficiency and strength of sol gel intermediate layer bonding](image)

The above results show that the unbonded area is quite low. Further studies are being carried out to modify the bonding process to eliminate the bubbles in the interfaces. There is good potential for the bonding techniques to be developed for integrating and packaging various micro/nanosystems with a wide range of materials including Si III–V semiconductor compounds, glass, and ceramic materials.

5.3 Anodic Bonding

Anodic bonding is widely used for bonding glass substrate to other conductive materials due to its good bond quality. It can serve as a hermetic and mechanical connection between glass and metal substrates or as a connection between glass and semiconductor substrates [3]. In anodic bonding, the substrates are typically heated to a temperature between 350 and 450 °C. A voltage of 4 to 10 V is applied across the glass and the other substrate to be bonded. Glass to glass wafer bonding has not been investigated extensively. However, glass to glass bonding has found useful applications in bio MEMS microfluidic displays and other areas due to the unique property of glass materials [7, 8].

Low-temperature bonding can avoid degrading or damaging pre-fabricated devices and integrated circuits. It can also minimize or eliminate bonding induced stress problems and warpage after cooling. Thus, materials with large differences in thermal expansion coefficients can be bonded together with better reliability.

Currently, much of wafer bonding research is focused on achieving strong wafer bonds at the lowest possible temperature [9, 7]. The bond quality generally deteriorates with decreasing bonding temperature. The bond strength is low and bubbles or cavities are prevalent at the interface.

In our study, an amorphous Si film was applied on the Si or glass wafer prior to bond with another glass wafer. Fig 8 shows the SAM micrographs for Si to glass, Si to glass and glass to glass bonded wafers under different temperatures at a voltage of 10 V bonding force of 10 N bonding time of 30 minutes and vacuum of 5 Pa. At low bonding temperatures (say 30 °C) and larger bubbles are found at the interfaces. With increased bonding temperature, the number of bubbles and the bubble size decrease noticeably. For Si to glass wafer bonding, it is difficult to eliminate the bubbles at the interface in the temperature range used in this study. It can also be seen that the bond efficiency is obviously improved with the assistance of an amorphous film. When the bonding temperature is higher than 50 °C and the voltage is higher than 10 volts, no bubbles are found. For glass to glass wafer bonding, when the bonding temperature is higher than 75 °C and the voltage is higher than 10 volts, no bubbles are found. The bonding temperature and the voltage have a significant influence on the bubbles. The unbonded area or bubbles are mainly attributable to gas entrapment between the mating surfaces of the two wafers. No bubbles arise from particle contamination; thus, indicating that the cleaning procedure is effective. Based on the above results, it can be seen that perfect Si to glass and glass to glass bonding can be achieved at temperatures no more than 30 °C.
Fig 8: Scanning acoustic micrographs (a, b, and c) Si to glass; (d, e, and f) a Si to glass; (g, h, and i) glass to glass. (a, d, and g: 5°C; b, e, and h: 5.5°C; c, f, and l: 3°C. Voltage is V bonding force is N bonding time is minutes and vacuum is Pa.

The bond strength is an important factor for bond quality and reliability. A high bond strength indicates that a good bond has been formed. Fig 9 shows the bond strength versus bonding temperature. The tensile strength of the bonded pairs is higher than MPa for Si to glass and glass to glass bonding and higher than MPa for the amorphous film coated silicon to glass bonding under all the bonding conditions.

The bond strength increases with an increase in the bonding temperature. It is believed that the glass is annealed during bonding process and the fracture strength of the glass is improved. The bond strength of the bonded pairs of amorphous silicon film coated silicon and glass is higher than that of the bonded pairs of bare silicon and glass especially at low bonding temperatures.

Fig 9: Bond strength versus bonding temperature.
6. Interconnection Techniques

6.1 Micro and Sub-micro Interconnection Technique
To achieve 3D systems, the bonding of the interconnect materials is another key technology. Soldering and adhesive bonding are the currently used joining methods [73 75]. Although soldering offers high yield and reliable connections, it requires complex and often environmentally unsound processes. Solder joining is not suitable for the pitches less than 5 μm as the micro solder joints may not be able to support the mechanical and electrical loading. The detrimental effect due to intermetallic growth is likely to be amplified in microjoints. Alternative joining processes using adhesives are limited by their lower reliability and relatively poor conductivity. Direct metal bonding is a method of joining two metal surfaces under ambient conditions without an intermediate layer (glue in between). It is a promising candidate for solving all the above problems. Metallurgical joints are highly reliable and can be applied to fine pitch interconnections with little or no melting during the process. Thermosonic and thermocompression bonding are popular processes for direct metal bonding. In 3D integration and packaging, low temperature and low-pressure bonding is always preferred to prevent problems such as thermal stress, defect generation, and the mechanical damage of components.

Metal bonds can be consistently and reliably formed between fragile wafers carrying sensitive devices at low temperatures and pressures. In our study, Au, Cu, and Ni are selected as the choices of metal joints. For Au, Au and Au-Ni bonding, the thermocompression bonding is employed. The bonding load is 5 g per bump, and the bonding time is 5 seconds. The influence of bonding temperature is studied from 300°C to 315°C. The result is shown in Fig. 1, which indicates the existence of a threshold bonding temperature. For Au, Au bonding below this critical value (515°C in this instance), there is nearly no joining as the joint strength is near zero. Above this critical point, small increase of temperature produces large improvement in joint strength. In other words, critical bonding temperature is the transition from “no bonding” condition to “bonding” condition. With the further increase of temperature, the joint strength increases steadily.

![Graph showing shear strength vs. bonding temperature](image)

Fig. 1 The effect of bonding temperature on shear strength

Au-Ni bonding also exhibits a critical bonding temperature in the bonding. No bonding transition and bonding is only possible above the critical temperature (515°C in this case). However, compared to Au-Au bonding, Au-Ni bonding has a lower critical bonding temperature. Under the same bonding condition, Au-Au did not bond at the temperature of 515°C, while the joint strength of Au-Ni bonding was 8.5g bump. Since the electroless nickel surface was covered by a layer of immersion gold, the bonding itself is still gold to gold bonding, which in all likelihood will be contaminated by similar ductile organic surface layers as in the earlier case of Au-Au bonding. The interfacial chemical state could be considered the same of Au-Ni as of Au-Au. Thus, the different critical bonding temperature would be more likely caused by the different interfacial mechanics.

Recently, the metallization schemes of vertical interlayer interconnects (VILICs) for 3D ICs have been demonstrated using direct wafer bonding. These techniques are based on the bonding of two wafers with their active layers connected through high aspect ratio vias, which serve as VILICs. One method is based on the optically adjusted bonding of a thinned (~5 μm) top wafer to a bottom wafer with an organic adhesive layer of polyimide (~3 μm) in between [76]. Interchip vias are etched through the ILD (inter level dielectric), the thinned top Si wafer and through the cured adhesive layer with an approximate depth of 50 μm prior to the bonding process. Fig. 2 (a) shows the interchip via made of chemical vapor deposited (CVD) TiN liner and CVD W plug provides a vertical interconnect (VILIC) between the uppermost metallization levels of both layers. The bonding between the two wafers (misalignment ≤ 5 μm) is done using a flip chip bonder with split beam optics at a temperature of 400°C.
A second technique relies on the thermocompression bonding between metal pads in each wafer [77]. In this method, Cu-Ta pads on both wafers serve as electrical contacts between the interchip via on the top thinned Si wafer and the uppermost interconnects on the bottom Si wafer. The Cu-Ta pads can also function as small bond pads for wafer bonding. Additionally, dummy metal patterns can be made to increase the surface area for wafer bonding. The Cu-Ta bilayer pads with a combined thickness of 7 nm are fused together by applying a compressive force at 4°C. This technique offers the advantage of a metal–metal interface that will lower the interface thermal resistance between the two wafers (and hence provide better heat conduction) and can be beneficial as a partial ground plane for lowering the electromagnetic effects.

Fig. Schematic of the wafer bonding techniques (a) with adhesive layer of polymer in between and (b) through thermocompression of copper metal.

At present, interconnection and packaging generally use metal or metal-based solders. With shrinkage in size of interconnects, bumps, and pitches especially for nanodevices and nanosystems, the current materials and methods may be no more suitable from the point of view of reliability. For example, at high current density, electromigration of copper atoms causes the formation of voids and eventual separation of interconnects leading to circuit failure. Electrical conductivity of copper interconnects also degraded at very small scales by electron scattering at surfaces and grain boundaries. Besides, the oxidation of metal at very small scales is a big concern for their applications.

So far, no viable techniques are available for high density interconnection and packaging especially for nanodevices and nanosystems.

6.2 Nano Interconnection Technique

Performance of micro nano devices and systems is being increasingly dominated by the interconnection and packaging due to decreasing bump size and pitch and increasing die size. Additionally, heterogeneous integration of different technologies in one single chip is becoming increasingly desirable for which planar (two-dimensional ICs) may not be suitable. 3D ICs and systems by short and vertical interlayer interconnections can significantly improve the performance and reduce wire limited chip area. Wiring or interconnection required to integrate or to package micro nano devices and systems must scale at the same rate as the devices and systems in order to take advantage of improvements in size and speed.

Interconnection and packaging will be one of the major challenges for development of nanosystems. Flip chip at chip level and wafer level have the advantages of having the lowest possible inductance per lead, highest frequency response speed as well as the lowest cross talk and simultaneous switching noise. Challenges arise when interconnection method of flip chip is gradually growing into the mainstream in the integration and packaging industry where the issue of size becomes increasingly critical for interconnection and pitches. Therefore, the development of a new type of flip chip interconnection material and technique is necessary to meet the ever-stringent requirements of mechanical thermal and electrical properties of interconnection when the interconnection dimension and pitch size are reduced to very fine scales.

With CNTs, outstanding electrical and mechanical properties [78, 84] they are suggested to be used as interconnect material for the future. CNTs have been compared with equivalent gold wires on their electrical performance. For example, the nanotubes with smaller diameter (8 nm) have lower resistance than Au wire whereas nanotubes with larger diameter (53 nm) have
higher contact resistance than Au wire. Both nanotubes have no degradation after a period of 35 hours at current density exceeding A cm.

In our study high density and aligned CNTs have been grown on metal pads on one wafer (Fig) which will be joined together with the metal pads on another wafer or substrate. With this concept nano interconnection can be realized.

![Image](Fig.png)

**Fig.** High density and aligned CNTs

**Conclusions**
Micro nanosystems are continuously being redefined as multifunctional systems with electronics, optical and mechanical functions and finding new applications in automotive chemical and biomedical products. Packaging and integration have to work around the diverse functional requirements and operating environments of micro nanosystems as well as the constant push for lower cost with system miniaturization. Semiconductor fabrication related processes are increasingly used in packaging and integration to keep pace with the rapid rate of high density miniaturization front end technology.

In this paper IC packaging MEMS/NEMS packaging and 3D integration and packaging are reviewed. A novel wafer level micro nanosystems integration and packaging concept has been proposed and the available key enabling technologies such as wafer boning techniques and micro nano interconnection have been described. It is expected that the new approach can make products multifunctional, lighter, smaller and cheaper.

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